IN THE CLAIMS

Please amend the claims to read as indicated herein.

1. (currently amended) An automated test equipment (ATE) comprising:

a plurality of per-pin testing units, wherein each of said plurality of per-pin testing units ~~is configurable~~ has circuitry for at least one of emitting a signal to, or receiving a signal from, a pin of a device under test (DUT) having a plurality of DUT pins, and wherein, during a testing sequence, said DUT is defined as (a) a first DUT core that represents a first functional unit of said DUT and (b) a second DUT core that represents a second functional unit of said DUT;

~~means for~~ an assigning component that assigns, during said testing sequence, a subset of said plurality of per-pin testing units to an ATE-port, for interfacing with said first DUT core via a subset of said plurality of DUT pins; and

~~means for~~ a programming component that obtains a specification for testing said first DUT core, prepares a program based on said specification, and programs said ATE-port with ~~a~~ said program ~~for testing said first DUT core~~,

wherein said program defines at least one of programming timing or a stimulus/response pattern, and specifies a per-pin timing in terms of sets of available waveforms for each of said plurality of per-pin testing units assigned to said ATE-port, and wherein each waveform represents a sequence of events of various types occurring at specified instances in time~~, and wherein said program is independent of a program for testing said second DUT core~~.

2. (currently amended) The automated test equipment of claim 1, wherein said ~~means for~~ assigning component comprises:

~~means for switching~~ a component that switches connections between one or more of said plurality of per-pin testing units and one or more of said plurality of DUT pins; and

~~means for controlling~~ a component that controls said switching in accordance with said assigning of said subset of said plurality of per-pin testing units.

3. (canceled)

4. (currently amended) The automated test equipment of claim 1, wherein said programming ~~means~~ component comprises at least one of:

~~means for specifying~~ a component that specifies cycle times of stimulus and response vectors for said ATE-port;

~~means for specifying~~ a component that specifies a pattern program for said ATE-port;

~~means for specifying~~ a component that specifies a per-pin vector data for each of said plurality of per-pin testing units assigned to said ATE-port; and

~~means for specifying~~ a component that specifies analogue set-up conditions for analogue pins of said ATE-port.

5. (currently amended) The automated test equipment of claim 1, wherein said programming ~~means~~ component comprises:

main pattern programs for implementing access protocols to said first DUT core.

6. (currently amended) The automated test equipment of claim 5, wherein said main pattern program comprises at least one of:

~~means for configuring~~ a component that configures said ATE-port for activating said subset of said plurality of per-pin testing units for accessing said first DUT core; and

~~means for selecting~~ a component that selects pattern data generated by pattern programs of said first DUT core during one testing sequence for testing said first DUT core.

7. (currently amended) The automated test equipment of claim 1, wherein said programming ~~means~~ component comprises:

~~means for specifying~~ a component that defines an alias mapping between said plurality of per-pin testing units for a plurality of ATE-ports, ~~for specifying~~ and specifies at least one of timing information and a pattern program of said ATE-port to apply for said plurality of ATE-ports for which said alias mapping is defined.

8. (currently amended) The automated test equipment according to claim 1, further comprising ~~means for specifying~~ a component that specifies overall test conditions for a test that concurrently operates on multiple ATE-ports.

9. (currently amended) The automated test equipment of claim 8, wherein ~~the specifying means~~ said component that specifies overall test conditions comprises at least one of:

~~means for determining~~ a component that determines a set of concurrently active ATE-ports during a defined testing sequence;

~~means for selecting~~ a component that selects ATE-port test conditions for one or more ATE-pins, for selecting an ATE-port timing setup for one or more ATE-pins;

~~means for specifying~~ a component that specifies global test conditions to express dependencies between pins of said DUT and said ATE; and

~~means for determining~~ a component that determines a multi-port pattern burst as a sequence of per-ATE-port pattern programs for each ATE-port.

10. (currently amended) A method for testing a device under test (DUT) with automated test equipment (ATE) having a plurality of per-pin testing units, wherein each of said plurality of per-pin testing units ~~is configurable~~ has circuitry for at least one of emitting a signal to, or receiving a signal from, a pin of said DUT, said method comprising:

defining, for a testing sequence, (a) a first DUT core that represents a first functional unit of said DUT, and (b) a second DUT core that represents a second functional unit of said DUT;

assigning, during said testing sequence, a subset of said plurality of per-pin testing units to an ATE-port, for interfacing with said first DUT core via a subset of said plurality of DUT pins; ~~and~~

obtaining a specification for testing said first DUT core;

preparing a program based said specification; and

programming said ATE-port with ~~a~~ said program ~~for testing said first DUT core~~, wherein said program defines at least one of programming timing or a stimulus/response pattern for said ATE-port, and ~~specifying~~ specifies a per-pin timing in terms of sets of available waveforms for each of said plurality of per-pin testing units assigned to said ATE-port, and wherein each waveform represents a sequence of events of various types occurring at specified instances in time~~, and wherein said program is independent of a program for testing said second DUT core~~.

11. (canceled)

12. (previously presented) The method of claim 10, wherein said defining at least one of programming timing and a stimulus/response pattern comprises at least one of:

specifying cycle times of stimulus and response vectors for said ATE-port;

specifying a pattern program for said ATE-port;

specifying per-pin vector data for each of said plurality of per-pin testing units assigned to said ATE-port; and

specifying analogue set-up conditions for analogue pins of said ATE-port.

13. (previously presented) The method according to claim10, further comprising:

specifying overall test conditions for a test that concurrently operates on multiple ATE-ports.

14. (previously presented) The method of claim 13, wherein specifying overall test conditions comprises:

determining a set of concurrently active ATE-ports during a defined testing sequence;

selecting ATE-port test conditions for one or more ATE-pins;

specifying global test conditions to express dependencies between pins of said DUT and said ATE; and

determining a multi-port pattern burst as a sequence of per-ATE-port pattern programs for each ATE-port.

15. (currently amended) A data media for storing computer instructions for automated test equipment, said data media comprising:

instructions for testing a device under test (DUT) with automated test equipment (ATE) having a plurality of per-pin testing units, wherein each of said plurality of per-pin testing units ~~is configurable~~ has circuitry for at least one of emitting a signal to, or receiving a signal from, a pin of said DUT, wherein said DUT includes a plurality of DUT pins;

instructions for defining, for a testing sequence, a first DUT core that represents a first functional unit of said DUT, and (b) a second DUT core that represents a second functional unit of said DUT;; and

instructions for assigning, during said testing sequence, a subset of said plurality of per-pin testing units to an ATE-port, for interfacing with said first DUT core via a subset of said plurality of DUT pins; ~~and~~

instructions for obtaining a specification for testing said first DUT core;

instructions for preparing a program based said specification; and

instructions for programming said ATE-port with a program for testing said first DUT core,

wherein said program defines at least one of programming timing or a stimulus/response pattern for said ATE-port, and specifies a per-pin timing in terms of sets of available waveforms for each of said plurality of per-pin testing units assigned to said ATE-port, and wherein each waveform represents a sequence of events of various types occurring at specified

instances in time~~; and wherein said program is independent of a program for testing said second DUT core~~.

16. (currently amended) An automated test equipment (ATE), comprising:

a plurality of per-pin testing units, wherein each of said plurality of per-pin testing units ~~is configurable~~ has circuitry for at least one of emitting a stimulus signal to, or receiving a response signal from, a pin of a device under test (DUT) having a plurality of DUT pins, and wherein, during a testing sequence, said DUT is defined as having a first functional unit and a second functional unit;

~~means for~~ an assigning component that assigns a subset of said plurality of per-pin testing units to an ATE-port for interfacing with said first functional unit via a subset of said plurality of DUT pins; and

~~means for~~ a programming component that obtains a specification for testing said first DUT core, prepares a program based on said specification, and programs said ATE-port with ~~a~~ said program for testing said first functional unit~~;~~

~~wherein said program is independent of a program for testing said second functional unit~~.

17. (currently amended) An automated test equipment (ATE), comprising:

a plurality of per-pin testing units, wherein each of said plurality of per-pin testing units ~~is configurable~~ has circuitry for at least one of emitting a stimulus signal to, or receiving a response signal from, a pin of a device under test, and wherein, during a testing sequence, said DUT is defined as having a first functional unit and a second functional unit;~~ and~~

~~an ATE port that receives a program~~ a programming component that obtains a specification for testing said first functional unit, prepares a program based on said specification, and interfaces with said first functional unit via a subset of said plurality of per-pin testing units to execute said program.

18. (currently amended) The ATE of claim 17,

wherein ~~said ATE port is a first ATE port, and~~ said subset is a first subset, said specification is a first specification, and said program is a first program, and

wherein said ~~ATE further comprises a second ATE port that receives a program~~ programming component obtains a second specification for testing said second functional unit, prepares a second program based on said second specification and interfaces with said second functional unit via a second subset of said plurality of per-pin testing units to execute said second program.

19. (currently amended) The ATE of claim 18, wherein said first program ~~for testing said first functional unit~~ is independent of said second program ~~for testing said second functional unit~~.

Please add the following claim, newly numbered as claim 20.

20. (new) The ATE of claim 18, wherein said first program and said second program are concurrently executed.